Long-lived, radiation-suppressed superconducting quantum bit in a planar geometry

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We present a superconducting qubit design that is fabricated in a 2D geometry over a superconducting ground plane to enhance the lifetime. The qubit is coupled to a microstrip resonator for readout. The circuit is fabricated on a silicon substrate using low loss, stoichiometric titanium nitride for capacitor pads and small, shadow-evaporated aluminum/aluminum-oxide junctions. We observe qubit relaxation and coherence times (T_1 and T_2) of 11.7 ± 0.2 μs and 8.7 ± 0.3 μs, respectively. Calculations show that the proximity of the superconducting plane suppresses the otherwise high radiation loss of the qubit. A significant increase in T_1 is projected for a reduced qubit-to-superconducting plane separation.

Superconducting qubits are a leading candidate for implementing scalable quantum information processing. A wide range of important experiments, such as violation of Bell's inequality [1–3], two qubit algorithms [3–5], and implementation of error correction codes [6, 7] have been demonstrated using these circuits. Since the first experiment by Nakamura *et al.* [8], significant effort has been expended to improve relaxation and coherence times, i.e. T_1 and T_2. For example, optimal biasing increased T_2 times [9] for charge qubits, and further improvements in both T_1 and T_2 were obtained using a device design that is inherently insensitive to charge noise, known as the transmon qubit [10, 11]. In these devices the readout is integral to the operation of the qubit. One widely used scheme for readout is the circuit quantum electrodynamics (cQED) architecture [12], where the qubit is dispersively coupled to a microwave resonator. In addition to its function as a measurement element, the resonator also acts as a filter of the electromagnetic environment. This reduces the number of decay channels for the qubit, thereby improving the qubit lifetime [13]. Typical lifetimes for a transmon qubit coupled to a 2D co-planar waveguide (CPW) resonator are on the order of a few μs, although lifetimes as long as 9.7 μs have been demonstrated by going to large area interdigitated capacitor plates [14], in order to reduce material loss.

Recent experiments have demonstrated considerably longer lifetimes for transmon qubits embedded in 3D high quality-factor cavities [15]. The cavity serves to both suppress radiation from the qubit and measure the qubit state. Using these cavity resonators, T_1 and T_2 times approaching 100 μs have been reported [16]. As pointed out in Ref. [15], these long lifetimes show that the Josephson junction is not the primary source of energy decay observed in the planar circuits. This indicates that, with proper engineering, planar Josephson circuits with long lifetimes should also be realizable.

In this work, we present an improved, 2D planar geometry for a qubit in a cQED architecture. Our design uses a microstrip resonator to read out the qubit, as shown in FIG. 1(a). This geometry has several benefits. Most importantly, the addition of a superconducting plane on the back side of the chip suppresses radiative loss from the qubit. It also allows for elimination of discontinuous ground planes on the top side of the chip that can cause stray resonances.

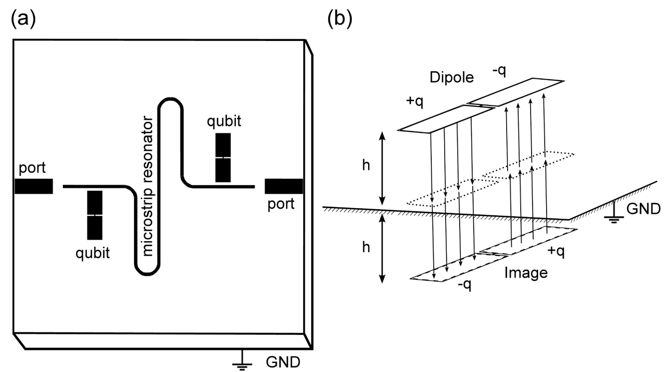

FIG. 1. (a) Chip layout. The device consists of two transmon qubits capacitively coupled to a microstrip resonator with a continuous superconducting ground plane on the backside. The resonator and the large qubit pads are made from TiN whereas the Josephson junction interconnecting the pads is made from Al/AlO$_x$/Al (b) Illustration of a dipole (the qubit in this case) at the distance h above a superconducting plane. The plane generates a mirror image of opposite charge (±q) which acts to suppress the radiation from the dipole.

The qubits are of the transmon type, i.e. the ratio of Josephson energy (E_J) to the charging energy (E_c) $\sim$ 100. The design used here is similar to that used by Paik *et al.* [15]. The circuits are fabricated primarily from stoichiometric titanium nitride (TiN) on intrinsic silicon (Si). Titanium nitride on Si is used because of its low microwave loss; CPW resonators made from TiN on Si have internal quality factors greater than 1×10^6 at single photon excitation [17]. The very low loss makes the TiN-Si system ideal for quantum circuits.

The TiN was deposited consecutively onto the top and bottom surfaces of a hydrogen terminated Si wafer (at

500 °C) using reactive sputter deposition [17]. The capacitor plates and the microstrip resonator were patterned into the top film with the use of photolithography. The structures were then fabricated in three steps. First, a small area was opened up where the junction was to be placed. This was done using a highly controllable CF_4-based reactive ion etch (RIE). In the second step, the remaining TiN circuit was etched using a SF_6-based RIE. The second step is necessary because, while the SF_6 etch produces low loss Si surfaces [18], it also produces large trenches (due to a high etch rate, 20:1, of Si:TiN in SF_6) that are not suitable for the junction area. In the third step, the Josephson junction interconnect between the capacitor plates was patterned with electron-beam lithography and formed by use of double angle Al evaporation and oxidation.

The sample was mounted in a Cu sample box with the TiN backplane electrically connected to the box. The ports (see Fig. 1 (a)), were wire-bonded to circuit boards leading to the coaxial connectors of the sample box. The sample was measured at the base temperature of a ^{3}He/^{4}He dilution refrigerator (≈ 20 mK). To characterize the two qubits (q1 and q2) on the chip, we used a pulsed, strong readout tone, resonant with the bare resonator frequency of 6.55 GHz [19]. The eigen-frequencies of the qubits were found to be $\nu_{q1} = 5.24$ GHz and $\nu_{q2} = 6.18$ GHz. We extracted a charging energy $E_c/h \approx 270$ MHz from the two photon Rabi oscillations of the 0→2 qubit transition and a coupling strength of $g/h \approx 150$ MHz from the dispersive shift of the cavity. From these, we obtain a Josephson energy of $E_J/h \approx 15$ GHz and $E_J/h \approx 21$ GHz for both q1 and q2.

The T_1 time for the qubits was measured by applying a π-pulse and measuring the state of the qubit as a function of delay time between the π- pulse and the readout pulse. Data are shown in FIG. 2 (a). Relaxation times of 11.7 ± 0.2 μs and 2.1 ± 0.1 μs for q1 and q2 respectively were extracted. The T_1 time of q2 is in good agreement with the expected Purcell limit. For q1, the expected Purcell limit is 20 μs. This is a factor of two greater than the observed T_1 time measured for this qubit.

The T_2 times were obtained from spin echo measurements and found to be 8.7 ± 0.3 μs and 4.6 ± 0.2 μs for q1 and q2 respectively (FIG. 2(b)). The T_2 time for q2 is found to be limited by its T_1 time. For q1 the T_2 is not limited by T_1, indicating that we have extra sources of decoherence affecting the qubits.

The large capacitor pad architecture of the qubit gives it a large dipole moment, allowing for strong coupling to the microstrip. However, this also increases the radiation of the bare qubit. In the 3D architecture, the radiation loss is suppressed by the cavity resonator. A more compact way to suppress this loss is by placing the qubit in close proximity (*i.e.*, a small fraction of the radiation wavelength) to a conductive plane, as illustrated in FIG. 1(b). The conducting plane generates a mirror image of the qubit dipole that radiates ∼180 degrees out of phase with the qubit dipole. The fields generated by the qubit and the image act to cancel each other, thereby suppressing the radiated power.

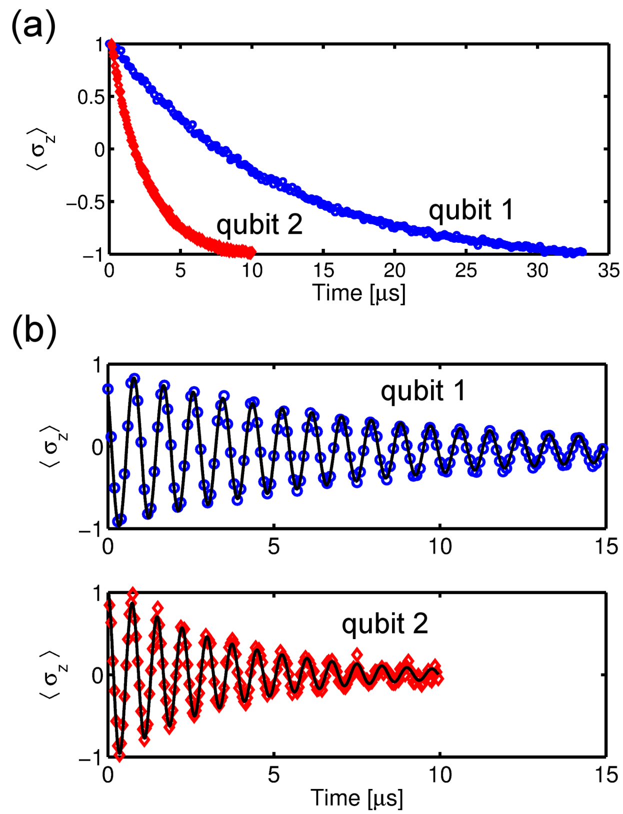

FIG. 2. (a) Measured relaxation time for the two qubits. We extract a T_1 time of 11.7 ± 0.2 μs and 2.1 ± 0.1 μs for qubit 1 and qubit 2, respectively. The T_1 time for qubit 2 agrees well with the expected Purcell limit, whereas T_1 for qubit 1 is shorter than expected. (b) Ramsey fringes for the two qubits. The extracted decoherence times T_2 are 8.7±0.3 μs and 4.6±0.2 μs for qubit 1 and qubit 2, respectively.

To quantify the effect of the conducting plane we use a finite element solver to calculate the time-averaged power flowing outwards from the dipole both with and without a superconducting plane. We find that the radiated power, $\overline{P}$, is suppressed by a factor of ∼100-400 in the far-field region for a substrate thickness of 350 μm over a 4-8 GHz frequency range. We estimate the effect of radiation loss on the relaxation time by defining a radiation resistance $R_{rad} = V^2/2\overline{P}$, where V is the port voltage driving the dipole. The radiation limited relaxation time $T_{rad} = R_{rad}C_s$ is then calculated, where C_s is the qubit shunt capacitance. Both the chip size and the substrate thickness affect the calculated T_1. The chip size dependence is shown in the inset of FIG. 3 where the radiation limit on T_1 for a substrate thickness of 350 μm is shown. For a chip size of 5×5 mm^2 we find $T_{rad} = 26$ μs, two orders of magnitude higher than the expected $T_{rad} = 0.13$

μs for a device without the conductive plane. Moreover, as shown in the main panel of Fig. 3. there is a significant increase in the calculated radiation-limit on T_1 as the substrate thickness decreases.

In this calculation, the effect of the sample box was not included. In order to evaluate the importance of the sample box for a qubit in close proximity to a superconducting ground plane, we measured the device with the lid removed from the box, thereby leaving the qubit and microstrip resonator exposed to the environment of the magnetic shielded, 20 mK stage of the dilution refrigerator. In these measurements we found T_1 and T_2 times of 9.7$\pm$0.5 and 8$\pm$0.5 μs, respectively. This shows that the sample box has minimal effect on the system.

Another important effect to consider is loss due to the materials. More specifically, potential sources of microwave loss at low powers and low temperatures are two level systems (TLSs) that are located primarily at the substrate-metal and substrate-vacuum interfaces [18, 20–22]. To quantitatively account for this, we calculated the filling factors of the different interfaces for qubit geometry and compared it to narrow gap CPW resonators previously studied [18]. We found a decrease of ≈ 5 and ≈ 10 in the filling factors of the Si-vacuum and TiN-Si interfaces respectively for the qubit geometry. From the extracted filling factors we calculate the TLS limit of the T_1 time to be between 35 μs up to 300 μs, depending on the loss distribution between the two interfaces. This is well above our measured T_1 time, hence we do not believe that the TLSs are is a limiting factor. A final materials concern is the use of the Al-TiN hybrid circuitry. We note that earlier work has shown that there is no measurable increase in the loss of lumped element TiN resonators at low temperatures due to the TiN-Al interface[23]. In fact, that work showed that there is a significant reduction of quasiparticle loss due to the higher T_C of the TiN relative to Al (4.5 vs. 1.1 K). These data, therefore, indicate that our qubit lifetimes are not yet limited by the materials.

In conclusion our measured T_1 time is in agreement with the expected T_1 from the combined contributions of the Purcell effect due to the readout resonator (20 μs) and the calculated radiation limit (26 μs). The measurement shows that the backside superconducting plane acts to suppress the radiation loss, and the simulations predict that decreasing the distance between the qubit and the plane can significantly increase T_1. Based on these measurements and simulations, we believe that 2D, planar cQED circuits with lifetimes comparable to those of their 3D counterparts can be achieved. In addition, having a local radiation suppression mechanism for the qubit makes it possible to bring in control lines to the qubit without reducing the qubit lifetime. This is a significant advantage compared to using 3D cavity resonators.

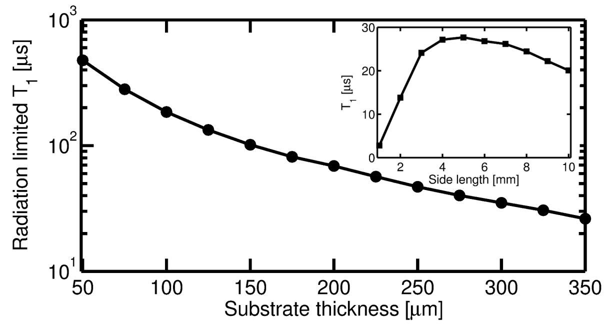

FIG. 3. Calculated relaxation time due to radiation losses for a qubit above a superconducting plane on the back side of the substrate. The spacing between the qubit and the plane is set by the substrate thickness. The inset shows the expected relaxation time as a function of chip side length for a 350 μm thick substrate.

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